REMARKS

This application has been reviewed in light of the Office Action dated January 4, 2007. Claims 1-10, 12-29, 30-32 and 33-48 are pending in the application. By the present amendment, claim 22 has been amended. Claim 11 stands cancelled without prejudice. No new matter has been added.

The Examiner's reconsideration of the rejection in view of the amendment and the following remarks is respectfully requested. It should be noted that the applicants are not conceding in this application that the amended claim in its prior form is not patentable over the art cited by the examiner, as the present claim amendment has been made only to facilitate expeditious prosecution of the application. The applicants respectfully reserve the right to pursue this and other claims in one or more continuations and/or divisional patent applications.

By the Office Action, claims 13-16, 21-27, 30 and 33-35 stand rejected under 35 U.S.C. §102 (b) as being anticipated by Pomerene et al. (U.S. Patent No. 4,679,141) (hereinafter Pomerene).

Pomerene discloses a branch predictor comprising a Pageable Branch History Table (PBHT) including a small, fast active area and a large, slow back-up area. An entry in either area of the PBHT contains a sequence of branch addresses and target addresses, referred to as "segments." The active area forwards segment (block) addresses to an instruction buffer, which retrieves the next instruction in its list from the segment (block address) in the cache (see Fig. 19). Every time a segment address is forwarded to an instruction buffer, the entry in the active area of the PBHT comprising the forwarded segment is deleted and a new segment is uploaded from the backup area (Pomerene, Column 13, lines 24-32).

The system of Pomerene determines which segment to upload from the backup area by utilizing an analyzer and stager. The analyzer examines the most recently uploaded segment and selects the segment corresponding to the exit (target) address of the the most recently uploaded segment (Pomerene Column 17, lines 32-68; Column 18, lines 1-38). The stager keeps the active area filled with segments predicted by the analyzer (Pomerene, column 18, lines 39-40). The analyzer does not reference a stored record of a sequence of BHT entries to determine the next segment uploaded into the active area.

The branch predictor disclosed in Pomerene does not disclose or suggest "a meta collector configured to collect and record look ahead context information . . . to enable . . . prefetching of the meta-information entries . . . based upon look ahead context information," as presented in claim 13. Moreover, Pomerene does not disclose or suggest "a meta-collector which collects and records . . .a sequence of accessed entries of a meta-structure corresponding to a cache line. . . ." as recited in claim 22.

"Look ahead context" includes "BHT entries that were recently referenced after the cache line was referenced." (Specification, p. 34, lines 10-13; p. 36, lines 19-20 to p. 37, line 1) (emphasis added). Look ahead context is used to predict branch locations to be prefetched during data processing. In one aspect of the present principles, the record is stored in a meta-collector, a memory storage device, a large meta-structure, a small meta-structure, or both the meta-collector and the memory storage device (Specification, 36 lines 3-13; p. 40, lines 7-10).

Figure 9 in the specification illustrates an example of collected look ahead context within a meta-collector. Each BA/TA pair in a cache line represents an entry of the BHT table that was accessed subsequent to when the cache line was referenced. The look

ahead context is a record of a sequence of BHT entries. In contrast, the segment of Figure 18 in Pomerene represents a single entry within a BHT.

It is important to note that in the specification a BHT entry was configured to have only one branch and target address pair for simplicity's sake (Specification, p. 21, lines 10-16). A single BHT entry may include many branch and target address pairs. The set of branch and target address pairs in a BHT entry correspond to a set of instructions obtained within a single fetch. A sequence of BHT entries corresponds to sets of instructions obtained in multiple fetches.

Pomerene does not disclose or suggest "a meta collector configured to collect and record look ahead context information . . . to enable . . . prefetching of the meta-information entries . . . based upon look ahead context information," as stated in claim 13. The analyzer in Pomerene predicts branch addresses based upon information contained within a single segment. Although the analyzer in Pomerene contains a sequence of segments, the sequence itself is not utilized for branch prediction. The analyzer does not predict branches utilizing a record of a sequence of BHT entries for branch prediction. Accordingly, claim 13 is believed to be patentable over Pomerene.

In addition, claim 22 is patentably distinguished over Pomerene, as Pomerene does not disclose or suggest "a meta-collector which collects and records . . .a sequence of accessed entries of a meta-structure corresponding to a cache line. . . ." The sequence of segments within the analyzer of Pomerene is transient in nature; it is changed every time a segment address is provided to the instruction buffer. Indeed, the sequence itself is not used at all in Pomerene. Moreover, the sequence of segments in Pomerene is not coupled to any cache line. Thus, claim 22 is believed to be patentable over Pomerene.

Therefore, for at least the reasons stated above, claims 13 and 22 are believed to be in condition for allowance. Furthermore, claims 14-16, 21, 23-27, 30 and 33-35 are believed to be in condition for allowance due at least to their dependencies from claims 13 and 22.

By the Office Action, claims 17-20 and 28-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pomerene in view of Zuraski (U.S. Patent No. 7,024,545) (hereinafter "Zuraski").

As discussed above, claims 13 and 22 are believed to be in condition for allowance. Thus, claims 17-20 and 28-29 are believed to be in condition for allowance due at least to their dependencies from claims 13 and 22, respectfully. Reconsideration of the rejection is respectfully requested.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to applicant's IBM Deposit Account No. 50-0510.

Respectfully submitted,

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